ALU design notes  
  
Please note that the red connections in this design symbolize four separate connections, and blue connections indicate separate connections.

I wanted to design my own shift register just for fun, so I did.

In the bit shifter only four tri-state buffers are present, but as the connections are

red this symbolizes 16 tri-state buffers.

Also, although the decoders have inverted output, the design calls for non inverted output.

I could only find chips with inverted output.  
  
  
  
  
  
Strangely the chip I used for the flags register does not have any read signals, so I am going to assume that its clock signal works as its enable.   
  
Because the status of the flag register needs to be saved in the case of an interrupt, the registers output will be connected to both the control unit and to the data in portion of the data-bus.  
The ZN flags will not be separate from the CO flags. They will be on the same chip.

I am thinking of representing each module with a different color to indicate that a connection attaches to that module in that way. To distinguish nibbles vs bytes, a connection will either start red or blue and then segment, to be continued in the new color. Since multisim doesn’t allow connections between two differently colored connections, this segment will be empty space.   
  
  
  
  
Here are some color coding ideas:  
  
Green: control unit  
Dark Yellow: ALU  
purple: interrupt module  
orange: data-bus  
  
  
  
I think that I am done with the preliminary design of the ALU, I might need to show my design to a teacher or professional to check that I haven’t left anything out but so far I am feeling good about it.